S. KAREN KHATAMIFARD

CONTACT INFORMATION

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RESEARCH INTERESTS

Application-domain specialized architectures, such as binary networks in *deep learning* and accelerated read aligners in *computational biology*. Impact of process technology on computing, resilient system design, **computer architecture**.

EDUCATION

University of Minnesota Twin Cities, USA

Ph.D. Candidate in Electrical Engineering (Computer Architecture) since 2013

- Advisor: Prof. Ulya R. Karpuzcu

Sharif University of Technology (SUT), Iran

B.S. in Electrical and Computer Engineering (Digital Systems) 2008-2013

- Thesis: Speech Recognition By Fuzzy Computing
- Advisor: Prof. Bagheri Shouraki

Young Scholar Club (YSC), Iran

A Three-Month Course on Informatics Olympiad (For top 40 students in Iran) 2007

- *Coursework*: Graph Theory, Algorithms, Programming

HONORS AND AWARDS

- ACM Turing Celebration **Travel Scholarship**, 2017
- **Departmental Fellowship**, University of Minnesota, 2013
- **National Elite Foundation** Fellowship for Undergraduates, 2008-2012
- **Ranked 103rd** out of 350000 undergraduate applicants in the National Universities Entrance Exam for B.Sc. degree, 2008
- **Bronze Medalist** of 10th National Olympiad in Informatics, 2007

PUBLICATIONS

[1] **S. Karen Khatamifard**, Longfei Wang, Weize Yu, Selcuk Kose, and Ulya R. Karpuzcu. ThermoGater: Thermally-Aware Distributed On-Chip Voltage Regulation. *Accepted for presentation in The 44th International Symposium on Computer Architecture (ISCA)*, June 2017.

[2] Filipe Betzel, **S. Karen Khatamifard**, Harini Suresh, David J. Lilja, John Sartori, , and Ulya Karpuzcu. Approximate Communication: Approximation Techniques for Communication Reduction in Parallel Systems. *ACM Computing Surveys*, April 2018.

[3] **S. Karen Khatamifard**, M. Hassan Najafi, Ali Ghoreishi, Ulya R. Karpuzcu, and David J. Lilja. On Memory System Design for Stochastic Computing. *IEEE Computer Architecture Letters (CAL)*, February 2018.

[4] **S. Karen Khatamifard**, Zamshed Chowdhury, Nakul Pande, Meisam Raziviyayn, Chris Kim, and Ulya R. Karpuzcu. A non-volatile near-memory read mapping accelerator. *arXiv preprint arXiv:1709.02381*, 2017.

[5] L. Wang, **S. K. Khatamifard**, O. A. Uzun, U. R. Karpuzcu, and S. Kose. Efficiency, Stability, and Reliability Implications of Unbalanced Current Sharing among Distributed On-Chip Voltage Regulators. *IEEE Transactions on Very Large Scale Integration Systems TVLSI*, November 2017.

[6] **S. Karen Khatamifard**, Ismail Akturk, and Ulya R. Karpuzcu. On Approximate Lock Elision. *ACM Transactions on Multi-Scale Computing Systems (TMSCS)*, November 2017.

[7] **S. Karen Khatamifard**, Meisam Raziviyayn, and Ulya R. Karpuzcu. BioArch: a reconfigurable hardware accelerator designed for bioinformatics workloads. *Accepted for presentation in the Genome Informatics Meeting 2017, Cold Spring Harbor Laboratory (CSHL)*, November 2017.

[8] Z. Chowdhury, J. D. Harms, **S. K. Khatamifard**, M. Zabihi, Y. Lv, A. P. Lyle, and J. P. Wang S. S. Sapatnekar, U. R. Karpuzcu. Efficient In-Memory Processing Using Spintronics. *IEEE Computer Architecture Letters (CAL)*, September 2017.

[9] **S. Karen Khatamifard**, Meisam Raziviyayn, and Ulya R. Karpuzcu. Binary Neural Networks for Hashing De novo Transcriptome Sequences. *Accepted for poster presentation in The Southern California Machine Learning Symposium (SoCal ML)*, September 2017.

[10] **S. Karen Khatamifard**, Nam Sung Kim, and Ulya R. Karpuzcu. VARIUS-TC: A Modular Architecture-Level Model of Parametric Variation for Thin-Channel Switches. *accepted for presentation in The 34th IEEE International Conference on Computer Design (ICCD)*, October 2016.

[11] Ismail Akturk, **S. Karen Khatamifard**, and Ulya R. Karpuzcu. On Quantification of Accuracy Loss in Approximate Computing. *accepted for presentation in 12th Annual Workshop on Duplicating, Deconstructing and Debunking colocated with ISCA*, July 2015.

CONFERENCE PRESENTATIONS

- BioArch: A Reconfigurable Hardware Accelerator Designed for Bioinformatics Workloads, Genome Informatics Meeting 2017, Cold Spring Harbor Laboratory (CSHL), Cold Spring Harbor, NY. November 2017
- ThermoGater: Thermally-Aware Distributed On-Chip Voltage Regulation, 44th International Symposium on Computer Architecture (ISCA), Toronto, Canada. June 2017
- A Modular Architectural Model of Parametric Variability for Emerging Switches, 34th IEEE International Conference on Computer Design (ICCD), Phoenix, AZ. October 2016
- On Quantification of Accuracy Loss in Approximate Computing, Workshop on Duplicating, Deconstructing and Debunking (WDDD, Co-located with ISCA), Portland, OR. June 2015

RESEARCH EXPERIENCE

An Accelerator for Bioinformatics Workloads Using Binarized Deep Neural Networks (since Spring 2017): A reconfigurable accelerator, including a novel *Binary Deep Neural Network kernel* to capture similarity between DNA sequences. [9, 7]

A Non-volatile Near-Memory Sequence Mapping Accelerator (since Fall 2016): A high-throughput accelerator for read mapping, based on a novel mechanism to capture similarity in *CAM arrays*. [4]

Mitigating Thermal Implications of On-Chip Regulators (Spring 2016 - Summer 2017): Demonstrating thermal implications of on-chip regulators under technology scaling. Introduced run-time practical polices to prevent thermal and voltage emergencies. [1, 5]

Improving Energy Efficiency by Approximate Data Communication Reduction (since Spring 2014): Exploring the energy efficiency benefits of eliminating synchronization in many-core systems, while keeping the accuracy loss at an acceptable level. [6, 2, 11]

Reliability Implications of Emerging Technologies (Fall 2013 - Summer 2016): Exploring micro-architectural implications of emerging technologies such as FinFETs. Developed *VARIUS-TC* tool for modeling the impact of parametric variation at architecture level. [10]

Rethinking Stochastic Computing Systems (Fall 2016 - Summer 2017): Introduced integration of analog memory with conventional stochastic systems to reduce the energy wasted in conversion units. [3]

TEACHING EXPERIENCE

Teaching & Laboratory Assistant, EE, SUT

- Computer Architecture 2011-2012
- Digital Design 2010-2011
- Principles of Electronics 2010

SERIVCE

- Reviewer of ICCD'17, TVLSI'17, IISWC'17, and ISCAS'17
- Head of the First Sharif Open Robotic Competitions, Tehran, Iran October 2012
- Executive head of the First Conference on Smart Grids, Tehran, Iran September 2010

COMPUTER SKILLS

- *Programming Languages:* C/C++, Python, Assembly
- *Miscellaneous:* Tensorflow, Matlab, R, Hspice, Cadence, LLVM, CUDA, OpenMP
- *Microarchitectural Simulators/Tools:* SniperSim & ESESC, McPAT, Hotspot, Voltpot, VARIUS
- *HDL:* Verilog